

IN THE CLAIMS

1-3. (Canceled)

4. (Currently Amended) A method for generating timing constraints, comprising the steps of:

describing a digital circuit using a hardware description language (HDL);
standard HDL;

constructing said digital circuit from said HDL description; and

replacing flip-flops in said digital circuit with negative delay elements;
elements.

breaking any feedback paths in the digital circuit by inserting dummy flip-flops clocked by clocks all having a period of substantially zero.

5. (Currently Amended) The method of Claim 4, wherein said negative-time elements are implemented by buffers having a delay $-T$, where T is a delay equal to a flip-flop's clock period less a typical predetermined flip-flop delay.

6. (Canceled)

7. (Currently Amended) The method of ~~Claim 6,~~ Claim 4, where said step of breaking said feedback paths is conducted so as to avoid breaking feedforward paths.

~~wherein cycles are only broken on backward paths.~~

8. (Currently Amended) The method of Claim 4, where said replacing step is conducted so that ~~wherein clocks and registers constructed have the property of slack equivalence, wherein~~ predetermined optimization goals at each gate are substantially the same as they would be if registers were already optimally distributed.

9. (Currently Amended) The method of Claim 5, wherein the actual value of T is set to a clock period of a flip-flop being replaced.

10. (Currently Amended) A method for generating timing constraints, comprising the steps of:

- describing a digital circuit using a hardware description language (HDL);
- constructing said digital circuit from said HDL description; and
- replacing flip-flops in said digital circuit with negative delay elements;

The method of Claim 4, further comprising the step of:

- where some of the negative delay elements comprise buffers, said buffers having a load capacitance using a buffer to replace a flip-flop, said buffer having a typical load capacitance, representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library.

11. (Currently Amended) A method for generating timing constraints, comprising operations of:

- describing a digital circuit using a hardware description language (HDL);
- constructing said digital circuit from said HDL description;
- replacing flip-flops in said digital circuit with negative delay elements;
- wherein said negative-time elements are implemented by buffers having a

- delay -T, where T is a delay equal to a flip-flop's clock period less a predetermined flip-flop delay;

The method of Claim 5, further comprising the step of:

- describing a value of T using a capacitance/delay curve representing a composite of gates in a target technology library, Q pins of flip-flops in said target technology library, and a series of increasingly powerful buffer trees;

- wherein said curve is first computed, then it is offset by setting a delay corresponding to a predetermined typical load capacitance to -T;

- where whereby a larger capacitive load results in a longer delay; and

whereby if a near-zero load is imposed a delay is $-(T + t)$, where t is a (positive) difference in delay between a predetermined typical load and a lesser load.

12. (Currently Amended) The method of Claim 4, further comprising the steps of:

after logic optimization, reinstalling registers in place of said negative-delay elements;

removing all dummy zero-clocked-cycle-breaking flip-flops;

applying a retiming process algorithm to reposition registers to optimize clock frequency and register count, said operation of applying the retiming process producing a retimed design; and

after retiming, applying further logic optimization to the retimed design.

after retiming, performing a second logic optimization pass to fine-tune said retimed design.

13-18. (Canceled)